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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/550,645	08/23/2006	Tominaga Koji	FUJ0002US	1944
23413	7590	02/05/2009	EXAMINER	
CANTOR COLBURN, LLP			MALEK, MALIHEH	
20 Church Street				
22nd Floor			ART UNIT	PAPER NUMBER
Hartford, CT 06103			2813	
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			02/05/2009	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

[usptopatentmail@cantorcolburn.com](mailto:usptopatentmail@cantorcolburn.com)

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/550,645	KOJI ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	MALIHEH MALEK	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 23 December 2008.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-6 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-6 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 23 September 2005 is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ .                                    |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____.   | 6) <input type="checkbox"/> Other: _____ .                        |

## **DETAILED ACTION**

This office action is in response to the RCE filed on 12/23/2008. Claims 1-6 are pending in this application. Applicant amended claims 1, 4, 5 and 6.

### ***Claim Objections***

1. Claims 3 and 6 are objected to as containing the following minor informalities:
  - Claims 3 and 6 are indistinct; it is not clear that how the high dielectric constant metal constitutional element relates to the high dielectric constant insulating film.
  - Regarding claims 3 and 6, the term "*high dielectric constant constitutional element*" is not introduced in the independent claim 1. Therefore, claims 3 and 6 can't depend on a term that was not introduced before.

Further clarification is requested.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in **Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966)**, that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: (**See MPEP Ch. 2141**)

- a. Determining the scope and contents of the prior art;
- b. Ascertaining the differences between the prior art and the claims in issue;
- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Evaluating evidence of secondary considerations for indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cabral, JR. et al. (Pub. No.: US 2006/0138603 A1), herein Cabral, in view of Doh et al. (Pub. No.: US 2006/0115993 A1 or KR 02-54606), herein Doh.

Regarding claim 1, Cabral teaches a semiconductor device comprising a silicon substrate; an interface layer provided on the silicon substrate, the interface layer comprising a metal silicate; a diffusion suppressing layer provided on the interface layer; and a high dielectric constant insulating film provided on the diffusion suppressing layer ([0077], “...other suitable lower layer materials include metal oxides or **metal silicates**. A **high-K dielectric layer** 56 selected from the group consisting of **hafnium oxide** and/or zirconium oxide...the dielectric materials comprising the multilayer structure with hafnium oxide and/or zirconium oxide are selected from the group including, but not limited to:  $Ta_2O_5$ ,  $TiO_2$ ,  $ZrO_2$ ,  $HfO_2$ ,  $Al_2O_3$ ,  $La_2O_3$ ,  $Y_2O_3$ , yttrium aluminate, lanthanum aluminate,

*lanthanum silicate, yttrium silicate, **hafnium silicate**, zirconium silicate, doped or undoped mixtures, layers or combinations thereof...,” and [0088]).*

However, regarding claim 1, Cabral does not explicitly teach a diffusion suppressing layer provided on the interface layer.

In the same field of endeavor, regarding claim 1, Doh teaches a diffusion suppressing layer provided on the interface layer ([0006]-[0009], “*...In various embodiments of the present invention, a method for treating one or more high dielectric layers of one or more integrated circuit devices involves the nitriding of a silicon substrate upon which the high dielectric layer is formed. The nitriding of the substrate may be performed, for example, by using a nitrogen plasma treatment, a thermal treatment in a nitrogen atmosphere, or a **thermal treatment of a nitrogen layer formed on the substrate**. Following nitriding, the silicon substrate and high dielectric layer are post treated by oxidizing the substrate to which the nitriding was applied, annealing the substrate to which the nitriding was applied, or by both oxidizing and annealing the substrate to which the nitriding was applied,*” to form high dielectric layers having superior mobility and interfacial characteristics (abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Cabral by incorporating the diffusion suppressing layer of Doh to form high dielectric layers having superior mobility and interfacial characteristics (Doh, abstract).

Regarding claim 3, Cabral teaches a semiconductor device wherein a high dielectric constant metal constitutional element in the constitutional element of the high dielectric constant insulating film is made the same as a part of the high dielectric constant constitutional element in the interface layer to prevent a reaction between the adjacent layers ([0077] and [0088]).

4. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada (Pub. No.: US 2002/0195643 A1) in view of Cabral, JR. et al. (Pub. No.: US 2006/0138603 A1), herein Cabral.

Regarding claim 4, Harada teaches a method for manufacturing a semiconductor device ([0001]) comprising: forming, on one surface of a silicon substrate 10, an initial layer 11b which is a high dielectric constant metal element film for being mutually diffused with silicon in the silicon substrate; forming a diffusion suppressing layer 11a ( $\text{Hf}_x\text{Si}_y\text{O}_2$ ) on the surface of the initial layer 11b ([0075]); performing heat treatment to allow the high dielectric constant metal element film of the initial layer to be mutually diffused with silicon in the silicon substrate 10, thereby forming an interface layer (silicon oxynitride film containing hafnium which prevents a reaction between the silicon substrate 10 and layer 11a); and forming a high dielectric constant insulating film on the surface of the diffusion suppressing layer ([0022]). The device structure of Harada is the same as the device claimed. It can be assumed that the device will inherently be

produced by the claimed process. See, for example, *In re King*, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986).

Regarding claim 4, Harada does not specifically teach forming an interface layer comprising a metal silicate.

In the same field of endeavor, regarding claim 4, Cabral teaches forming an interface layer comprising a metal silicate ([0077], “*...other suitable lower layer materials include metal oxides or metal silicates. A high-K dielectric layer* 56 *selected from the group consisting of hafnium oxide and/or zirconium oxide...the dielectric materials comprising the multilayer structure with hafnium oxide and/or zirconium oxide are selected from the group including, but not limited to: Ta<sub>2</sub>O<sub>5</sub>, TiO<sub>2</sub>, ZrO<sub>2</sub>, HfO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, La<sub>2</sub>O<sub>3</sub>, Y<sub>2</sub>O<sub>3</sub>, yttrium aluminate, lanthnaum aluminate, lanthanum silicate, yttrium silicate, hafnium silicate, zirconium silicate, doped or undoped mixtures, layers or combinations thereof...*” and [0088]) to fabricate a device with superior electrical properties with minimal flat band voltage shift, an appropriate threshold voltage, low inversion thickness, and enhanced mobility ([0009]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Harada by incorporating the metal silicate layer as an interface layer to fabricate a device with superior electrical properties with minimal flat band voltage shift, an appropriate threshold voltage, low inversion thickness, and enhanced mobility (Cabral, [0009]).

Regarding claim 5, Harada teaches a method for manufacturing a semiconductor device ([0001]) comprising: forming, on one surface of a silicon substrate, an initial layer which is a high dielectric constant metal element film for being mutually diffused with silicon in the silicon substrate; forming a diffusion suppressing layer on the surface of the initial layer; forming a high dielectric constant insulating film on the surface of the diffusion suppressing layer ([0075]); and performing heat treatment to allow the high dielectric constant metal element film of the initial layer to be mutually diffused with silicon in the silicon substrate, thereby forming an interface layer comprising a metal silicate ([0022]). The device structure of Harada is the same as the device claimed. It can be assumed that the device will inherently be produced by the claimed process. See, for example, *In re King*, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986).

Regarding claim 5, performing heat treatment after or before forming the high dielectric constant insulating film is an obvious alternative since selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results; *In re Burhans*, 154 F.2d 690 USPQ 330 (CCPA 1946); *In re Gibson*, 39 F2d 975, 5 USPQ 230 (CCPA 1930). MPEP 2144.04.

Regarding claim 5, Harada does not specifically teach forming an interface layer comprising a metal silicate.

In the same field of endeavor, regarding claim 5, Cabral teaches forming an interface layer comprising a metal silicate ([0077], “...other suitable lower layer materials include metal oxides or **metal silicates**. A high-K dielectric

*layer 56 selected from the group consisting of **hafnium oxide** and/or zirconium oxide...the dielectric materials comprising the multilayer structure with hafnium oxide and/or zirconium oxide are selected from the group including, but not limited to: Ta<sub>2</sub>O<sub>5</sub>, TiO<sub>2</sub>, ZrO<sub>2</sub>, HfO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, La<sub>2</sub>O<sub>3</sub>, Y<sub>2</sub>O<sub>3</sub>, yttrium aluminate, lanthnaum aluminate, lanthanum silicate, yttrium silicate, **hafnium silicate**, zirconium silicate, doped or undoped mixtures, layers or **combinations thereof...**" and [0088]) to fabricate a device with superior electrical properties with minimal flat band voltage shift, an appropriate threshold voltage, low inversion thickness, and enhanced mobility ([0009]).*

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Harada by incorporating the metal silicate layer as an interface layer to fabricate a device with superior electrical properties with minimal flat band voltage shift, an appropriate threshold voltage, low inversion thickness, and enhanced mobility (Cabral, [0009]).

5. Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cabral, JR. et al. (Pub. No.: US 2006/0138603 A1), herein Cabral, in view of Doh et al. (Pub. No.: US 2006/0115993 A1 or KR 02-54606), herein Doh, as applied above, and further in view of Bai (Pub. No.: US 2001/0013629 A1).

Regarding claim 2, the previous combination remains as applied to claim 1 above.

However, regarding claim 2, the previous combination does not teach a semiconductor device wherein the interface layer has an equivalently converted SiO<sub>2</sub> thickness of 1.0 nm or smaller.

In the same field of endeavor, regarding claim 2, Bai teaches a semiconductor device wherein the interface layer has an equivalently converted SiO<sub>2</sub> thickness of 1.0 nm or smaller ([0020] and table I) to increase the capacitance of a gate dielectric without decreasing the performance of the device ([0012]). Bai discloses the claimed invention except for the exact value of the SiO<sub>2</sub> thickness of 1.0 nm or less. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have an interface layer having equivalently converted SiO<sub>2</sub> thickness of 1.0 nm or less, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Regarding claim 6, Harada teaches a semiconductor device wherein a high dielectric constant metal constitutional element in the constitutional element of the high dielectric constant insulating film is made the same as a part of the high dielectric constant constitutional element in of the interface layer to prevent a reaction between the adjacent layers ([0075]).

### ***Response to Arguments***

6. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MALIHEH MALEK whose telephone number is (571)270-1874. The examiner can normally be reached on Mon-Fri, 8:30-6pm ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571)272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jan.31, 2009

/M. M./  
Examiner, Art Unit 2813

/Matthew S. Smith/  
Supervisory Patent Examiner, Art Unit 2823